광범위한 부하 적용을 위한 25kW급 고주파 위상천이 PWM 풀브리지 DC/DC 컨버터 개발

배상인, 정우철, 박장훈, 태민우, 류홍제
중앙대학교

Development of a 25kW high-frequency phase-shift PWM full-bridge DC/DC converter for a wide range of load applications

Sang-In Bae, Woo-Cheol Jeong, Jang-Hun Park, Min-Woo Tae, Hong-Je Ryoo
Chung-Ang University

ABSTRACT

This paper suggests the implementation of a 25kW phase-shifted full bridge converter (PSFB) operating at high frequency. The operating frequency was set as 500kHz and a full bridge switch module was applied to the PSFB for high power density, which contains a state-of-the-art semiconductor device technology. Since the applicability to a wide range of load conditions is one of the important concerns, a zero-voltage detection gate driver was also applied to the PSFB. The enhanced high-efficiency operating range across various load conditions was verified through simulations and experiments. According to the content, this paper is organized as follows: 1) the overall scheme of the proposed converter, including controller, switch module, and rectifier. 2) high efficiency derived from the zero-voltage detection gate driver and the consideration of the rectifier's resonance. 3) comparison of switching loss through simulations and experiments.

1. Introduction

The implementation of microgrids utilizing renewable energy necessitates the deployment of systems such as electric vehicle (EV) charging facilities and energy storage systems (ESS) with sufficient power. This growing reliance on these systems is significantly driving the demand for modules containing high-efficiency, high-density DC/DC converters.

However, existing modules have significant bulk and weight, which limit the ability to build a power bank of sufficient capacity with them and their applicability to a wide range of load conditions is also a major consideration. In response, the development of modules with exceptional power density and universality, as proposed in this paper, can significantly increase the capacity of each charging facility, which can lead to the advancement of the related industry.

This paper aims for the module which has a maximum output of 500V 50A with an input voltage of 800V. With a 25kW capacity, the module utilizes a phase-shifted pulse width modulation (PSPWM) full bridge converter enabling broad load applicability and simplified control.

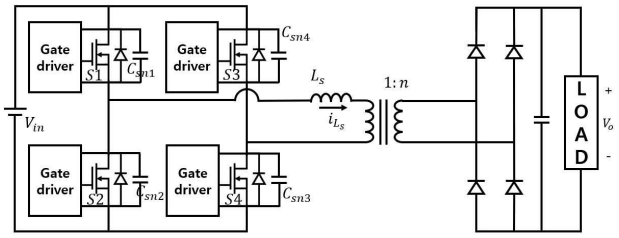
This paper describes the circuit design considering high-frequency operation of 500kHz which enabled high power density, with the switch module, the latest semiconductor technology is adopted. Not only this meticulous design, but the utilization of specialized gate drivers implemented to enhance the ZVS range of the converter, is detailed. As a final point, considerations regarding resonance in the rectifier stage are also incorporated in this paper in terms of efficiency.

The designed charger module has a volume of nearly 2 liters, which means the power bank utilizing this module will have a power capacity of 10MW in just 800L. It is expected that the various branches explored in this paper, aimed at achieving notable power density, will significantly contribute to the future development of power banks.

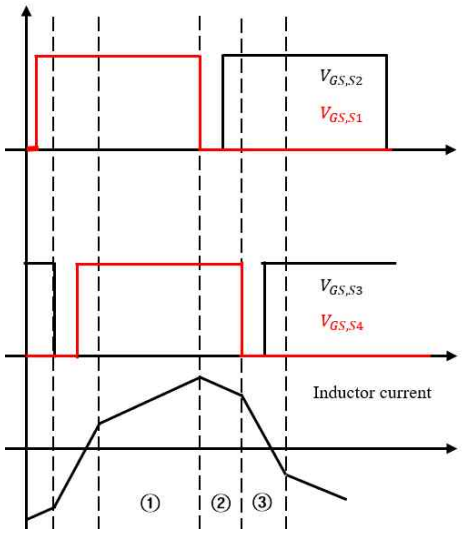
2. Analysis of the PSPWM full bridge converter

Fig. 1(a) shows the schematic diagram of the PSPWM full bridge converter, and its operation modes are detailed in Fig. 1(b). Initially, during ①, S1 and S4 are turned on, facilitating the transfer of power from the primary side to the secondary side. Upon turning off S1, making the end of the power transfer, the output capacitance of the leading leg is charged and discharged, which, in turn, the current flows through the anti-parallel diode of S2 and S4 in ②. As a result, only the output voltage is applied, independent of primary-side power, causing a reduction in inductor current. In ③, S4 is turned off and the output capacitance of the lagging leg undergoes charging and discharging, so if the current is insufficient, the voltage across the switch can not be completely discharged, leading to hard switching.

This is especially exacerbated when light load conditions, where the power delivery bandwidth shrinks, producing inadequate current and hindering the achievement of ZVS, are coupled with fixed dead time. To address this challenge, Section 3.1 of this paper introduces the utilization of a



(a)



(b)

그림 1 풀브릿지 컨버터 (a) 회로도 (b) 동작 모드

Fig. 1 Full bridge converter (a) schematic diagram (b) operation mode

zero-voltage detection gate driver. This approach allows for the dynamic adjustment of the dead time, thereby enhancing operational efficiency and facilitating ZVS under diverse load conditions.

3. Design of the proposed 25kW PSPWM full bridge converter

3.1 Zero-voltage detection gate driver

Fig. 2 shows the schematic diagram of a zero-voltage detection gate driver. This gate driver controls the turn-on speed of the main switch (S1) by regulating the rate at which the capacitor (C1) connected to the gate-source of the turn-on MOSFET (Son) is charged. Thus, to optimize the performance, the resistor (R2) connected in series to C1 must be smaller than the resistor (R1) connected parallel to C1. This configuration facilitates the achievement of maximum dead time and effective zero-voltage detection. Additionally, the maximum dead time can be adjusted according to the value of the R5, enabling enhanced performance for active load applications.

The zero-voltage detection gate driver is not only beneficial to actively responding to various load conditions, but it is also advantageous for the use of snubber capacitors. Typically, the use of snubber capacitors to mitigate turn-off losses has been constrained, as they can

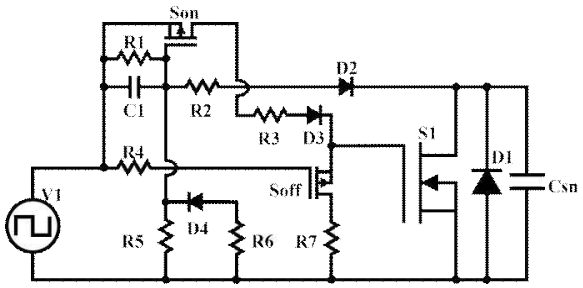
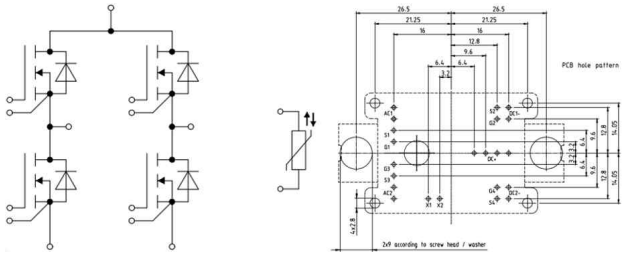


그림 2 영전압 감지 게이트 드라이버 회로도

Fig. 2 Schematic diagram of the zero-voltage detection gate driver



(a) (b)

그림 3 SiC 스위치 모듈 (a) 회로도 (b) 구조도 [1]

Fig. 3 SiC switch module (a) schematic diagram (b) block diagram

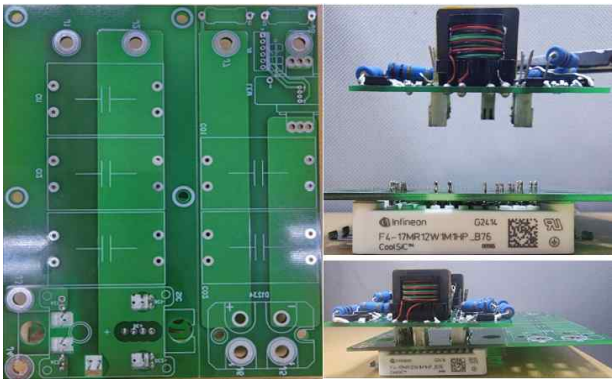
lead to suboptimal ZVS conditions. However, active dead time adjustment provides enough time for the switch to turn on, thereby allowing for the incorporation of larger snubber capacitors.

3.2 Converter design for high-frequency operation

The SiC switch module was used as a crucial component for high-frequency operation. As shown in the schematic and block diagram in Fig. 3, this module is designed as a highly compact full-bridge configuration, which enabled the converter to minimize inductance while maximizing compactness, optimizing performance for a high-frequency.

The design of the converter PCB was also precisely optimized for high-frequency operation, as it is closely related to inductance. To balance and minimize inductance, the components were arranged symmetrically and connected with minimized pattern lengths. As shown in the PCB design in Fig. 4(a), the gate driver, controller, switch module, and rectifier were all integrated into a single PCB. Notably, to further reduce gate loop inductance, the gate driver was directly connected to the switch module via a designed terminal for the gate-source connection, which is illustrated in Fig. 4(b).

Lastly, the transformer played a pivotal role in achieving high power density within the converter design. To enhance compactness, a planar transformer was employed in lieu of a toroidal transformer. Ferrite was chosen as the core material to ensure that the maximum core flux density, induced by the peak winding current, remains below the saturation flux density, and in terms of a sufficient current capacity, the Litz wire was chosen. Moreover, optimal design considerations for the window area were made, taking into



(a) (b)

그림 4 (a) PCB 판 (b) Gate driver와 Switch module 연결

Fig. 4 (a) PCB board (b) Connection between the gate driver and the switch module

account the turn ratio and winding fill factor to accommodate the dimensions of the Litz wire effectively. These design strategies collectively fostered a setting that is well-suited for high-frequency applications.

4. Simulation and experimental result

The use of fixed dead time can pose challenges under varying load conditions. In light load conditions, the fixed dead time may be insufficient due to the limited energy stored in the inductor, which requires adequate time for the voltage across the MOSFET to discharge. Conversely, merely increasing the fixed dead time is not a viable solution, as it can lead to a reversal in the polarity of the inductor current when the MOSFET is in the off state. This reversal causes the voltage across the MOSFET to charge, resulting in increased turn-on losses. Therefore, a balanced approach to dead time management is essential to optimize performance across different operational conditions.

As a response, Fig. 5(a) and 5(b) show simulation results utilizing a zero voltage detection with 800V input voltage. The black vertical line is the point at which it crosses the gate threshold voltage. As demonstrated, hard switching is prevented by adopting the zero-voltage detection gate driver. Moreover, the dead time is actively adjusted in accordance with the load conditions. To summarize, this flexibility facilitates the realization of soft switching under varying operational conditions, thereby enhancing the overall efficiency and performance of the converter.

Additionally, resonance in the rectifier during the free-wheeling period contributed to further power losses. By reducing the parasitic capacitance of the rectifier diode, overall efficiency was improved.

5. Conclusion

This paper described the implementation of a 25kW PSPWM full-bridge converter with a switching frequency of 500kHz for a high power density. As a condition to be applied to such a high frequency properly, the cutting-edge switch module was adopted, and the PCB and transformer were also designed precisely. On top of that, the converter could achieve significant improvements in applicability and efficiency by extending the ZVS range through the zero-voltage detection gate driver while simultaneously minimizing secondary-side resonances.

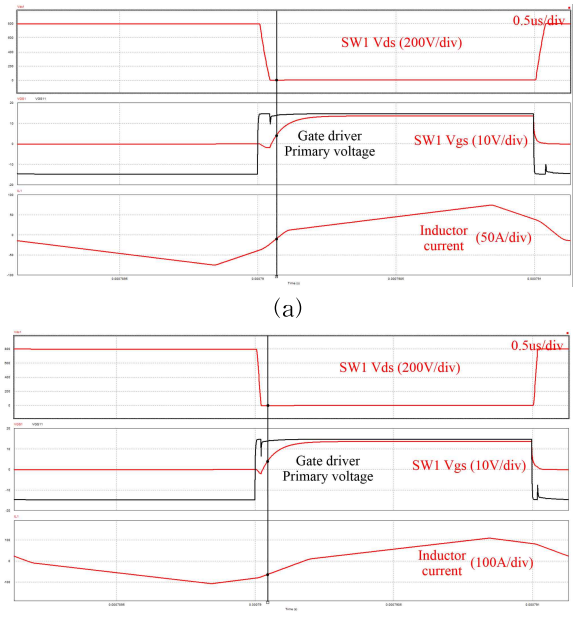


그림 5 800V 입력전압의 PSPWM 풀브릿지 컨버터 PSIM 영전압 감지 시뮬레이션 (a) 정격부하 (b) 경부하

Fig. 5 PSPWM full bridge converter PSIM zero voltage detection simulation with 800V input voltage (a) rated load (b) light load

Reference

[1] Infineon technologies AG, "F4-17MR12W1M1HP_B76.", pp. 12-13, September 2022. F4-17MR12W1M1HP_B76