Novel Modular Multilevel Converter with Middle Submodule for Fault-Tolerant Operation

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ABSTRACT

This paper proposes a novel modular multilevel converter (MMC) with middle submodule (SM), where the SM capacitor voltage fluctuation is reduced and the reliability of system is enhanced. A middle SM is placed between the upper and lower arms, which is controlled to generate high-frequency voltages to mitigate the low-frequency power fluctuation in both arms. In addition, once SM failure is detected, the middle SM is reconfigured to operate like a healthy SM, which can substitute the faulty SM. The effectiveness of the proposed topology has been confirmed through the simulation results.

1. Introduction

MMC is regarded as one of the promising topologies for medium-voltage applications due to their scalability, modularity, and low output voltage distortion [1]. However, the main issue is that the SM capacitor voltage fluctuation is proportional to output current amplitude and inversely proportional to output frequency [1]. To reduce this, different control methods and topology modifications have been introduced [1]-[3].

A sinusoidal-wave injection method has been presented [1], where high-frequency common-mode voltage (CMV) and circulating current are injected into the phase legs for rebalancing the power deference between the upper and lower arms. Therefore, SM capacitor voltage fluctuations have been reduced. However, the CMV is imposed on the AC-side.

A modification of MMC topology has been introduced to alleviate the SM capacitor voltage fluctuation [2], where the capacitors of the top and bottom SMs are connected via two cables. However, the SM capacitor voltage fluctuation is still large. Another modified MMC has been presented [3], where a middle SM with six switching devices and one capacitor are inserted between upper and lower arms. However, the switching devices could be potentially reduced and the functionality of the middle SM could be extended.

In this paper, a novel MMC with middle SMs is proposed. A middle SM consists of five switching devices and one capacitor, which is controlled to generate high-frequency voltages. Besides, the AC-circulating current is injected into legs; thus, the SM capacitor voltage fluctuation can be reduced. In addition, the middle SM can substitute a faulty SM in the upper or lower arms when the faulty SM is detected. To confirm the feasibility of the proposed topology, a simulation of the proposed converter system is carried out.

2. Novel MMC with Middle SM

2.1 Circuit configuration

Fig. 1(a) shows the circuit configuration of the proposed topology, where one leg consists of two arms and one middle SM. One arm is comprised of identical half-bridge SMs and inductor. The middle SM is placed between two arms. In Table I, switching states of middle SM are listed, where “1” and “0” indicate the ON and OFF states of the switch, respectively, and “x” represents either one. According to operating modes, corresponding switches are used to configure middle SM. There are three operating modes such as mitigation of SM capacitor voltage fluctuation, substitution of a faulty SM in the upper or lower arms.

![Circuit configurations](image)

**Table I**: Switching states of middle SM

<table>
<thead>
<tr>
<th>Operating modes</th>
<th>S₁</th>
<th>S₂</th>
<th>S₃</th>
<th>S₄</th>
<th>S₅</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mitigation of SM capacitor voltage fluctuation</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Substitution of faulty SM in upper arm</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Substitution of faulty SM in lower arm</td>
<td>1</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

2.2 Mitigation of SM capacitor voltage ripple

In the operating mode for mitigation of SM capacitor voltage fluctuation, S₂ is always turned on, which leads to the circuit configuration of middle SM as shown in Fig. 1(b). S₃ and S₅ are controlled with the same gating values, which are complementary to the switches S₁ and S₅, respectively. Based on switching states, $v_{yx}$ is the output voltage of middle SM in the upper arms, $v_{yz}$ is the output voltage of middle SM in the lower arms. In addition, a high-frequency voltage, $v_h = V_h \sin(\omega_c t)$, is injected into both arms with opposite polarity to $v_{yx}$ and $v_{yz}$. The arm voltages ($v_{xL}$ and $v_{zL}$) and output terminal ($v_{yx}$ and $v_{yz}$) of middle SM are expressed, respectively, as:

$$v_{ix} = 0.5V_{dc} - v_x - v_z,$$

$$v_{iz} = 0.5V_{dc} + v_x + v_z,$$

$$v_{yx} = v_x,$$

$$v_{yz} = v_z.$$
\[ v_{c^-} = -v_{c^+}. \] (4)

To reduce the low-frequency power fluctuation in arms, the AC-circulating current \( (i_{ab}) \) is injected into legs besides the DC-circulating current \( (i_{d}) \). The upper and lower arms currents, \( i_{ab} \) and \( i_{d} \), are expressed as:
\[
\begin{align*}
  i_{ab} &= 0.5i_a + i_c = 0.5i_a + i_{ab},
  \quad (5) \\
  i_a &= -0.5i_a + i_c = -0.5i_a + i_{d}. \quad (6)
\end{align*}
\]

In arms, \( i_{ab} \) is controlled in phase with \( v_{oa} \), which helps to mitigate the low-frequency power fluctuation and rebalance the power difference between both arms.

2.3 Ability of fault-tolerant operation

During the operation of mitigating the SM capacitor voltage fluctuation, a fault detection and fault localization are employed to bypass a faulty SM and continue the converter operation without significant degradation of performance. If a faulty SM is detected and identified, the middle SM is reconfigured as the half-bridge SM to substitute the faulty SM. Then, the proposed topology is reconfigured just like the conventional MMC.

Fig. 1(c) shows the reconfiguration of middle SM when a faulty SM is detected in the upper arm. Based on the switching states, \( S_3 \) and \( S_6 \) are turned on, and \( S_4 \) is turned off. The switches \( S_1 \) and \( S_5 \) are controlled to function as a half-bridge SM, which maintains the desired voltage of the upper arm.

In addition, if the faulty SM is detected in the lower arm, the middle SM is reconfigured to substitute the faulty SM as shown in Fig. 1(d). To operate as a half-bridge SM, the switches \( S_2 \) and \( S_4 \) are employed. \( S_1 \) and \( S_5 \) are turned on, and \( S_6 \) is turned off.

3. Simulation Results

To verify the effectiveness of the proposed topology, the simulation test is carried out for three-phase system with four SMs per arm. The DC-link input voltage is 7000 V, the rated SM capacitor voltage is 1750 V, the SM capacitance is 2 mF, the frequency value of the injected components is 500 Hz and the modulation index is 0.6.

Fig. 2 shows performance of the proposed topology when the faulty SM occurs in the upper arm. From \( t = 0.1 \) s to \( t = 0.3 \) s, the middle SM is configured to reduce the SM capacitor fluctuation. Thus, the SM capacitor voltage fluctuation is mitigated with 165 V in a peak-to-peak value as shown in Fig. 2(b). It can be seen that the SM voltage includes high-frequency components besides the fundamental frequency one. Fig. 2(c) illustrates the capacitor voltages of middle SMs, where they are controlled at the reference (1750 V) with low ripple. At \( t = 0.3 \) s, when the faulty SM is detected in the upper arm, the middle SM is reconfigured to substitute the faulty SM. Then, the converter is operated as the conventional MMC. Since the SM 1 in the upper arm fails, it is bypassed and its capacitor voltage is not changed as shown in Fig. 2(b). In the operation of as the conventional MMC, the SM capacitor voltage fluctuation becomes higher (240 V) due to no mitigation of low-frequency power fluctuation.

Fig. 3 shows the performance when the faulty SM exists in the lower arm. It is similar to Fig. 2, where the mode of reducing the SM capacitor fluctuation is applied from \( t = 0.1 \) s to \( t = 0.3 \) s. After that, when the SM 1 in the lower arm has failure, the middle SM is reconfigured to substitute the faulty SM. Then, the converter is operated as the conventional MMC.

4. Conclusions

This paper has proposed a novel MMC with middle SM, where the SM capacitor voltage fluctuation has been reduced and the ability of fault-tolerant operation has been featured. A suggested

Fig. 2. Performance of the proposed topology when the faulty SM exists in the upper arm.

Fig. 3. Performance of the proposed topology when the faulty SM exists in the lower arm.

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References