A Robust Harmonic Elimination Method for Three Phase Grid-Connected Inverters Using a Digital Lock-in Amplifier and FLL

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Abstract
The output quality of the grid connected inverters has become a serious concern in this era due to the increase in use of distributed generation and renewable energy sources. Though the THD of the inverter is limited less than 5% by the standards such as IEEE-519, it is very difficult to achieve it over the wide load range. The poor quality of the inverter output is mainly attributed to the incomplete harmonic compensation caused by the inaccurate harmonic detection. In this paper a robust harmonic elimination method for three phase grid-connected inverters using a Digital Lock-in Amplifier (DLA) and DLA based Frequency Locked Loop (FLL) is proposed. Due to the outstanding characteristics of the DLA the harmonics can be detected with high accuracy and compensated completely. In addition the grid frequency variation is detected by the DLA based FLL and used to detect the harmonic accurately under the grid frequency variation. The validity of the proposed method is proved by both PSIM simulations and experiments with a 10kW grid connected inverter. THD of the inverter output is 4.62% at 10% load.

1. Introduction
In recent years, the Distributed Generations (DGs) using renewable energy sources are increasing at rapid rate to cope with the worldwide problems such as the depletion of the fossil fuel and climate change. The Grid-Connected Inverters (GCIs) are typically used as the interfaces to connect the renewable energy based source to the grid. Since the inverters convert the DC to AC by using Pulse Width Modulation (PWM) the output of the GCI can hardly be a perfect sinusoidal waveform. Therefore the harmonics are also injected to the grid as well as the fundamental component when the GCI is connected to the grid. The standard such as IEEE 519-2014 limits the harmonics to be injected to the grid so as to protect the equipment from the problems caused by the harmonics in the grid.

So far many kinds of research have been conducted to improve the output quality of the GCIs. In the GCI the harmonics generated by the PWM can be simply eliminated by employing a passive filter such as an LCL filter [1]. However, the harmonics are also generated by the harmonics already present in the grid. Since the fundamental current controller can hardly eliminate the high frequency component, the harmonics appears at the output of GCIs [2-3]. There is an approach to eliminate the current harmonics by employing PR controllers [4]. However, it is difficult to tune the PR controller for each harmonic and its performance gets worse when the grid frequency varies. The SOGI-based harmonic compensation method in the synchronous reference frame proposed in [5], but it is not able to compensate all of the harmonics perfectly due to the nonideal characteristics of the SOGI. Recently, a method to use the Digital Lock-In Amplifier has been introduced [6] and it shows an outstanding performance in detecting and compensating the harmonics. However, since the FLL was not employed the performance of the harmonic compensation gets deteriorated when the grid frequency varies.

In this paper a novel harmonic compensation method using Digital Lock-in Amplifiers (DLAs) and DLA based FLL(Frequency Locked Loop) is proposed for the three phase GCI. Since the FLL is adopted the harmonic compensation can be achieved perfectly under the varying grid frequency condition. The validity of the proposed system is prove by the experiments with a 10kW prototype GCI.

2. DLA Based Harmonic Elimination using FLL
The proposed DLA based harmonic elimination method using FLL is showing in Fig. 1. As already discussed in [6], DLA can
extract the harmonic information with high accuracy. After the Digital Lock-in Amplifiers, a simple PI controller is used to convert the current error into voltage duty. The reconstructed harmonics are fed back to the current controller for the harmonics elimination. One disadvantage of the DLA is that its accuracy deteriorates when the frequency of the signal to be detected changes. Therefore the frequency of the reference signal to be multiplied to the grid current needs to be changed according to the grid frequency to maintain the accuracy of detection.

2.1 DLA Based Harmonic Elimination Technique

Fig. 1 shows the full circuit diagram including harmonic elimination part. It should be noted that the harmonics need to be detected from each phase separately since the harmonics at each phase may be different.

As shown in Fig. 1, the reference signal for DLA is generated by a Digital Signal Processor (DSP) with the phase information of the grid from the DLA-based FLL to explained in the next section. The dc value of a specific harmonic after the Low Pass Filter (LPF) can be expressed by (1).

\[ x = \frac{V_a}{2} \cos(\theta_a - \theta_{ref}) \]

\[ y = \frac{V_a}{2} \sin(\theta_a - \theta_{ref}) \]

(1)

Where, \( \theta_a \) and \( \theta_{ref} \) represents the phase of the input signal and reference signal, respectively, theta information, whereas \( V_a \) is the peak value of the input signal. Then, a PI controller is used for the harmonic compensation DLA. The output of the PI is used to reconstruct the compensation signal as shown in (2).

\[ H_{\text{DSF}} = A_a \cos(m\theta_{\text{FLL}} + \theta_{\text{ref}}) \]

(2)

Where, \( A_a \) is the magnitude and \( \theta_{\text{ref}} \) is the phase information of the mth harmonic.

2.2 DLA based Frequency Locked Loop

In the proposed harmonic elimination method DLA is used and 60Hz reference signal is generated by the DSP with an arbitrary phase and detects the phase difference between the reference signal and the same frequency component in the input signal. Therefore when the grid frequency changes then the detection performance of the DLA gets deteriorated. In this paper DLA based Frequency Locked Loop (FLL) is proposed to track the grid frequency and generates the reference signal for the DLA with the actual grid frequency as shown in Fig. 2.

![Fig. 2. Proposed Lock-in Amplifier based Frequency Locked Loop](image)

The output signal produced by DLA includes a DC component and a double line frequency ripple. In order to filter out the AC component a 2nd order Notch-filter incorporated with a first order LPF is employed to improve the dynamic response of the FLL. When \( f_{\text{in}}=60Hz \), \( f_{\text{ref}}=60Hz \) and \( \theta_{\text{ref}} = \theta_a \), and both input signal and reference signal are of the same frequency with a normalized magnitude \( V_{\text{in}} = 1 \), then equation can be written as,

\[ V_{\text{in}} = \frac{1}{2} \left[ \cos(2\pi(0) + 0) - \cos(2\pi(20) + 0) \right] \]

(3)

\[ V_{\text{in}} = \frac{1}{2} \left[ \sin(2\pi(0) + 0) + \sin(2\pi(20) + 0) \right] \]

(4)

The DLA output after the filter is a pure DC which provides the magnitude of the input signal for frequency extraction. Then the derivative function is applied to get the frequency change.

\[ \Delta f_{\text{FLL}} = \frac{\Delta \theta}{2\pi dt} \]

(5)

After that, a PI controller is used to reduce the steady-state error. The small deviation of the frequency calculated by (5) is added to 60Hz (reference frequency). From the extracted grid frequency \( f_{\text{FLL}} \) the \( \theta_{\text{FLL}} \) can be calculated by taking the integration as (6).

\[ \theta_{\text{FLL}} = \int \frac{2\pi f_d t}{0} \]

(6)

One critical factor of the FLL is its capability to track the input signal frequency within 160ms as suggested by IEEE-1547. The faster settling time brings a great advantage for the GCI system. An additional advantage of the proposed DLA based FLL method is that it is not affected by the dc offset present in the input signal.

3. Simulation and Experiment Results

In order to prove the validity of the proposed method simulations as well as the experiments are carried out with a 10kW prototype three-phase grid-connected inverter. Here, the dc-link voltage is 400Vdc. The output voltage of the GCI is 220Vrms at 60Hz and the switching frequency of the inverter is 10KHz.

First of all the performance of the frequency tracking with the proposed DLA based FLL is demonstrated by PSIM simulation. Fig. 3 is the simulation results to show the frequency tracking performance of the DLA-based FLL. In this simulation the grid frequency was varied from 60Hz to 58Hz and from 60Hz to 62Hz. As shown in Fig. 3 and the frequency tracking time is 151ms which satisfied the IEEE-1547.

![Fig. 3. Dynamic Response of the Proposed DLA Based Frequency Locked Loop](image)

Fig. 4(a) and (b) shows the PSIM simulation of grid-injected currents from the inverter without DLA-harmonic elimination method. Fig. 4(a) represents the three-phase currents waveform at 100% load (10kW power). It can be seen from Fig. 4(b) that \( 5^\text{th} \), \( 7^\text{th} \) and \( 9^\text{th} \) harmonics are the main reasons for the distorted current while the other odd harmonics have less contribution. Fig. 4(c) and (d) shows the simulation waveform of the grid currents injected by the three-phase inverter with DLA based harmonic elimination method and DLA-based FLL.

Fig. 4(c) represents the three-phase currents waveform at 10kW. It can be noticed that most dominant odd harmonics are eliminated by using the proposed method. In Fig. 4(d) it is clearly shown that all the harmonics are compensated perfectly as proved by the following FFT results.

The experiments are carried out with the prototype 10kW three phase GCI and the control of the inverter is performed through a digital signal processor (TMS320F28335). The DLA harmonic
A robust harmonic compensation method with DLA based harmonic elimination technique and DLA based FLL is proposed and its validity is proved by the simulation and experiments with a 10kW GCI. With the proposed technique the 3rd, 5th and 7th harmonics have been successfully eliminated and less than 5% current THD was achieved even at 10% rated load (1kW). The proposed DLA based FLL meets the IEEE suggestion in terms of dynamics and it can be used to eliminate the harmonics from the output of the GCI.

4. Conclusion

A robust harmonic compensation method with DLA based harmonic elimination technique and DLA based FLL is proposed and its validity is proved by the simulation and experiments with a 10kW GCI. With the proposed technique the 3rd, 5th and 7th harmonics have been successfully eliminated and less than 5% current THD was achieved even at 10% rated load (1kW). The proposed DLA based FLL meets the IEEE suggestion in terms of dynamics and it can be used to eliminate the harmonics from the output of the GCI.

Reference


